CLAIMS

The invention claimed is:

1. A semiconductor processing patterning method, comprising:

forming a first layer of resist over a substrate;

forming a second layer of resist over the first layer of resist;

exposing overlapping portions of the first and second resist layers to actinic energy effective to change solubility of the exposed portions versus the unexposed portions of each of the first and second resist layers in a developer solution; and

after the exposing, developing the first and second layers of resist with the developer solution to form a mask pattern over the substrate comprising the first and second resist layers, the first resist layer of the mask pattern having opposing sidewalls in at least one cross section and the second resist layer of the mask pattern having opposing sidewalls in the one cross section, at least a portion of the opposing sidewalls of the first resist layer being received laterally inward of at least a portion of the opposing sidewalls of the second resist layer in the one cross section.

2. The method of claim 1 wherein the first and second layers of resist are of different compositions as initially formed.

3. The method of claim 1 wherein the first layer of resist is photosensitive to electromagnetic radiation at a wavelength of no greater than about 325 nm.

4. The method of claim 1 wherein the second layer of resist is formed on the first layer of resist.

5. The method of claim 1 wherein both the first layer of resist and the second layer of resist comprise negative resist.

6. The method of claim 1 wherein both the first layer of resist and the second layer of resist comprise positive resist.

7. The method of claim 1 wherein the actinic energy comprises UV radiation.

8. The method of claim 1 wherein the actinic energy comprises an e-beam.

9. The method of claim 1 wherein the developing comprises etching an exposed portion of the first layer of resist faster than an exposed portion of the second layer of resist.

10. The method of claim 1 wherein the first layer of resist comprises at least one of 1-methoxy-2-propanol and ethyl lactate the second layer of resist comprises at least one of cyclohexanone and 2-heptanone.

11. The method of claim 1 wherein the developer solution comprises TMAH.

12. The method of claim 1 wherein the first layer of resist has a thickness which is less than a thickness of the second layer of resist.

13. The method of claim 1 wherein the first layer of resist has a thickness which is less than a total thickness of all layers received over the first layer of resist.

14. The method of claim 1 wherein the first layer of resist has a thickness which is less than or equal to about 50% of a total thickness of the first layer of resist and all layers received over the first layer of resist.

15. The method of claim 1 wherein the first layer of resist has a thickness which is less than or equal to about 25% of a total thickness of the first layer of resist and all layers received over the first layer of resist.

16. The method of claim 1 wherein the first layer of resist has a thickness which is less than or equal to about 10% of a total thickness of the first layer of resist and all layers received over the first layer of resist.

17. The method of claim 1 wherein the first layer of resist has a thickness which is less than or equal to about 5% of a total thickness of the first layer of resist and all layers received over the first layer of resist.

18. The method of claim 1 further comprising after the developing, etching material of the substrate using the mask pattern as a mask.

19. The method of claim 1 wherein the opposing sidewalls of the first resist layer are at least partially curved in the one cross section.

20. The method of claim 1 wherein the opposing sidewalls of the first resist layer and the opposing sidewalls of the second resist layer are of different shapes in the one cross section.

21. The method of claim 1 wherein an entirety of the opposing sidewalls of the first resist layer in the one cross section are recessed laterally inward of the opposing sidewalls of the second resist layer in the one cross section.

22. A semiconductor processing patterning method, comprising:

forming a first positive resist layer over a substrate;

forming a second positive resist layer over the first positive resist layer, the first and second positive resist layers being different in composition, the first positive resist layer having greater solubility in a developer solution than does the second positive resist layer at least after exposure to actinic energy effective to increase solubility of each of the first and second positive resist layers in the developer solution;

exposing overlapping portions of the first and second positive resist layers to said effective actinic energy; and

after the exposing, developing the first and second positive resist layers with the developer solution to form a mask pattern over the substrate comprising the first and second positive resist layers, the developing solution removing the exposed portions of the first positive resist layer at a faster rate than removing the exposed portions of the second positive resist layer effective to form the mask pattern to have opposing sidewalls of the first positive resist layer in at least one cross section at least a portion of which are recessed laterally inward of at least a portion of opposing sidewalls of the second positive resist layer in the one cross section.

23. The method of claim 22 wherein the first positive resist layer is photosensitive to electromagnetic radiation at a wavelength of no greater than about 325 nm.

24. The method of claim 22 wherein the second positive resist layer is formed on the first positive resist layer.

25. The method of claim 22 wherein the actinic energy comprises UV radiation.

26. The method of claim 22 wherein the actinic energy comprises an e-beam.

27. The method of claim 22 wherein the first positive resist layer comprises 1-methoxy-2-propanol and the second positive resist layer comprises cyclohexanone and 2-heptanone.

28. The method of claim 22 wherein the developer solution comprises TMAH.

29. The method of claim 22 wherein the first positive resist layer has a thickness which is less than a thickness of the second positive resist layer.

30. The method of claim 22 wherein the first positive resist layer has a thickness which is less than a total thickness of all layers received over the first positive resist layer.

31. The method of claim 22 wherein the first positive resist layer has a thickness which is from about 25% to about 50% of a total thickness of the first positive resist layer and all layers received over the first positive resist layer.

32. The method of claim 22 wherein the first positive resist layer has a thickness which is from about 5% to about 10% of a total thickness of the first positive resist layer and all layers received over the first positive resist layer.

33. The method of claim 22 wherein the first positive resist layer has a thickness which is less than about 5% of a total thickness of the first positive resist layer and all layers received over the first positive resist layer.

34. The method of claim 22 further comprising after the developing, etching material of the substrate using the mask pattern as a mask.

35. The method of claim 22 wherein the opposing sidewalls of the first positive resist layer are at least partially curved in the one cross section.

36. The method of claim 22 wherein an entirety of the opposing sidewalls of the first positive resist layer are recessed laterally inward of the opposing sidewalls of the second positive resist layer in the one cross section.

37. A semiconductor processing patterning method, comprising:

forming a second composition resist layer over a different first composition resist layer;

exposing overlapping portions of the first and second composition resist layers to actinic energy effective to initiate formation of a mask pattern having a second mask block over a first mask block, wherein solubility of the first mask block is greater than solubility of the second mask block in a developer solution; and

developing the first and second composition resist layers with the developer solution under conditions effective to remove the material of the first mask block at a faster rate than removing the material of the second mask block and form the mask pattern.

38. The method of claim 37 wherein the first composition resist layer is photosensitive to electromagnetic radiation at a wavelength of no greater than about 325 nm.

39. The method of claim 37 wherein the second composition resist layer is formed on the first composition resist layer.

40. The method of claim 37 wherein the second mask block is formed on the first mask block.

41. The method of claim 37 wherein the actinic energy comprises UV radiation.

42. The method of claim 37 wherein the actinic energy comprises an e-beam.

43. The method of claim 37 wherein both the first composition resist layer and the second composition resist layer comprise negative resist.

44. The method of claim 37 wherein both the first composition resist layer and the second composition resist layer comprise positive resist

45. The method of claim 37 wherein the first composition resist layer comprises 1-methoxy-2-propanol and the second composition resist-layer comprises cyclohexanone and 2-heptanone.

46. The method of claim 37 wherein the developer solution comprises TMAH.

47. The method of claim 37 wherein the first mask block has a thickness which is less than a thickness of the second mask block.

48. The method of claim 37 wherein the first composition resist layer has a thickness which is less than a total thickness of all layers received over the first composition resist layer.

49. The method of claim 37 wherein the first composition resist layer has a thickness which is less than or equal to about 50% of a total thickness of the first composition resist layer and all layers received over the first composition resist layer.

50. The method of claim 37 wherein the first composition resist layer has a thickness which is less than or equal to about 25% of a total thickness of the first composition resist layer and all layers received over the first composition resist layer.

51. The method of claim 37 wherein the first composition resist layer has a thickness which is less than or equal to about 10% of a total thickness of the first composition resist layer and all layers received over the first composition resist layer.

52. The method of claim 37 wherein the first composition resist layer has a thickness which is less than or equal to about 5% of a total thickness of the first composition resist layer and all layers received over the first composition resist layer.

53. The method of claim 37 wherein the mask pattern comprises opposing sidewalls of the first mask block in at least one cross section at least a portion of which are recessed laterally inward of at least a portion of the opposing sidewalls of the second mask block in the one cross section.

54. The method of claim 53 wherein the opposing sidewalls of the first mask block are at least partially curved in the one cross section.

55. The method of claim 53 wherein the opposing sidewalls of the first mask block and the opposing sidewalls of the second mask block are of different shapes in the one cross section.

56. The method of claim 53 wherein an entirety of the opposing sidewalls of the first mask block in the one cross section are recessed laterally inward of the opposing sidewalls of the second mask block in the one cross section.

57. The method of claim 53 further comprising after the developing, etching material of the substrate using the mask pattern as a mask.

58. A semiconductor construction comprising a semiconductor substrate having a patterned resist mask received thereon, the resist mask comprising a first composition resist portion and a different second composition resist portion received over the first composition resist portion, the first composition resist portion having opposing sidewalls in at least one cross section and the second composition resist portion having opposing sidewalls in the one cross section, at least a portion of the opposing sidewalls of the first composition resist portion being recessed laterally inward of at least a portion of the opposing sidewalls of the second composition resist portion.

59. The semiconductor construction of claim 58 wherein the second composition resist portion is received on the first composition resist portion.

60. The semiconductor construction of claim 58 wherein both the first composition resist portion and the second composition resist portion comprise negative resist.

61. The semiconductor construction of claim 58 wherein both the first composition resist portion and the second composition resist portion comprise positive resist.

62. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than a thickness of the second composition resist portion.

63. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than a total thickness of all layers received over the first composition resist portion.

64. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than or equal to about 50% of a total thickness of the first composition resist portion and all layers received over the first composition resist portion.

65. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than or equal to about 25% of a total thickness of the first composition resist portion and all layers received over the first composition resist portion.

66. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than or equal to about 10% of a total thickness of the first composition resist portion and all layers received over the first composition resist portion.

67. The semiconductor construction of claim 58 wherein the first composition resist portion has a thickness which is less than or equal to about 5% of a total thickness of the first composition resist portion and all layers received over the first composition resist portion.

68. The semiconductor construction of claim 58 wherein the opposing sidewalls of the first composition resist portion are at least partially curved in the one cross section.

69. The semiconductor construction of claim 58 wherein the opposing sidewalls of the first composition resist portion and the opposing sidewalls of the second composition resist portion are of different shapes in the one cross section.

70. The semiconductor construction of claim 58 wherein an entirety of the opposing sidewalls of the first composition resist portion in the one cross section are recessed laterally inward of the opposing sidewalls of the second composition resist portion in the one cross section.